CLAIMS

What is claimed is:

1. A method for facilitating analysis of a signal, comprising:

identifying a period of said signal;

adjusting a sample rate so that an integer number of sample intervals equals said period of said signal;

configuring a cyclic counter to reset according to said integer number; and

capturing ensembles of data samples of said signal that are respectively defined by successive resets of said cyclic counter.

2. The method of claim 1 further comprising:

coherently averaging captured ensembles without post-processing to time shift each sample of said captured ensembles.

3. The method of claim 1 wherein said adjusting is performed using a programmable frequency synthesizer.

4. The method of claim 1 wherein said adjusting is performed using a programmable rate digital resampler.

5. The method of claim 1 further comprising:

generating a trigger signal for said capturing in response to a reset of said cyclic counter.

6. The method of claim 5 further comprising:

adjusting a reset point of said cyclic counter to delay or advance said trigger signal relative to said signal.

7. The method of claim 1 further comprising:

initializing said cyclic counter using a trigger mechanism.

8. The method of claim 1 further comprising:

adjusting timing of said sample rate by a fraction of a period of said sample interval.

9. The method of claim 1 wherein said period of said signal defines an interval between a repetition of a phase of said signal.

10. The method of claim 1 wherein said period of said signal defines an interval between a repetition of signal stochastic properties.

11. A system for processing a signal that possesses a period, comprising:

an analog-to-digital (A/D) converter for sampling said signal;

sample capture circuitry for obtaining samples of said signal at a sample rate such that an integer number of sample intervals equals said period;

cyclic counter logic that counts each captured sample and comprising a programmable modulus set to said integer number; and

wherein said sample capture circuitry is operable to output time aligned ensembles of captured samples that are defined by respective resets of said cyclic counter logic.

12. The system of claim 11 further comprising:

a programmable frequency synthesizer for varying a sampling rate of said A/D converter.

13. The system of claim 11 further comprising:

digital resampling circuitry disposed between said A/D converter and said sample capture circuitry for programmably varying a rate that samples are provided to said sample capture circuitry.

14. The system of claim 13 wherein said digital resampling circuitry adjusts timing of communication of samples between said A/D converter by a fraction of a programmably variable rate of said digital resampling circuitry.

15. The system of claim 11 further comprising:

a trigger mechanism configured to initialize said cyclic counter logic.

16. The system of claim 11 wherein said period defines a repetition between a phase of said signal.

17. The system of claim 11 wherein said period defines a repetition between signal stochastic properties.

18. A system for processing a signal that possesses a period, comprising:

means for providing samples of said signal at a sample rate, wherein an integer number of sample intervals defined by said sample rate equals said period;

means for cyclically counting samples provided by said means for providing such that said means for cyclically resets after said integer number; and

means for outputting time aligned ensembles of samples defined by respective resets of said means for cyclically counting.

19. The system of claim 18 wherein said means for providing samples comprises:

a programmable rate digital resampler.

20. The system of claim 18 wherein said means for providing samples comprises:

a digital to analog converter driven by a clock defined by a programmable frequency synthesizer.